Abstract

An ADC circuit includes a multiplexer, a calibration circuit, one or more ADC banks, and a calibration ladder, all on an integrated circuit. The calibration resistor ladder is enabled during a calibration phase, and disabled during normal operation. When enabled, the calibration resistor ladder provides a calibration reference signal. Also, the multiplexer provides the calibration reference signal to one or more ADC banks during a calibration phase, and provides an analog input signal to the ADC banks otherwise. The calibration circuit is arranged to provide one or more adjustment signals to the ADC banks to calibrate the ADC banks in response to one or more comparator output signals from the ADC banks.

Customer No.: 38845